PVP 12

Code: EC6T1

III B.Tech - II Semester – Regular Examinations - May 2015

VLSI DESIGN
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Marks: 5x14=70

Answer any FIVE questions. All questions carry equal marks

1 a) List out the differences between Enhancement and Depletion MOSFETs. 7 M

b) Develop and explain the fabrication process of Enhancement n-channel MOSFET. 7 M

2 a) Extract the relation between I_d versus V_{ds}, when an nMOS is operated in Non-saturation region. 7 M

b) With necessary derivation, determine pull-up to pull-down ratio for an NMOS inverter driven by another NMOS inverter through one or more pass transistors. 7 M

3 a) With a neat sketch, construct the layout diagram of CMOS NOR Gate. 7 M

b) Enumerate the λ -based design rules to draw the layouts of CMOS circuits. 7 M

4 a) Explain the issues and remedies involved in driving large capacitive loads. 7 M

b) Write about the main parameters involved in finding the delay of inverters. 7 M

5 a) Write about the scaling limitations due to sub-threshold currents in a MOSFET. 7 M

b) Construct 4:1 Multiplexer using Pass transistor switch logic. 7 M

6 a) Compare PLA and PAL in view of their design and architecture. 7 M

b) Develop flowchart for VLSI full custom design. 7 M

7 a) Construct and explain Xilinx 4000 CLB. 7 M

b) List out the features of Altera CPLDs. 7 M

8 a) With suitable stick diagrams, explain Stuck-at-1(SA1) and stuck-at-0(SA0) methods. 7 M

b) Write about Design strategies for testing of VLSI circuits. 7 M